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Claims

[c1] 1. A digital-to-analog converter comprising:

a band gap voltage regulator;

a voltage divider comprising a plurality of tunneling n-type field effect transistors (NFETs) connected to said band gap voltage regulator;

a multiplexer connected to said voltage divider;

a digital decoder connected to said multiplexer;

an operational amplifier connected to said multiplexer; and

an input binary word component connected to said digital decoder;

wherein outputs of said digital decoder are input into said operational amplifier and converted as analog output.

[c2] 2. The digital-to-analog converter of claim 1, wherein said multiplexer comprises any of a NFET, a p-type field effect transistor (PFET), and a combination thereof.

[c3] 3. The digital-to-analog converter of claim 1, further comprising a capacitor connected to said operational amplifier.

[c4] 4. The digital-to-analog converter of claim 3, wherein said multiplexer and said capacitor comprise an oxide of at least 5 nm in thickness.

[c5] 5. The digital-to-analog converter of claim 1, further comprising a binary-weighted tunneling current device connected to said digital decoder.

[c6] 6. The digital-to-analog converter of claim 5, wherein said tunneling current device outputs tunneling current, wherein said tunneling current is adjusted in proportion to a binary weight of said input binary word component.

[c7] 7. The digital-to-analog converter of claim 5, further comprising:

a node coupled to said digital decoder;

at least one current supply field effect transistor (FET) coupled to said node; and

an output FET operable for supplying a current proportional to a current of said current supply FET;

wherein said current supply FET is operable for maintaining voltage on said node constant.

[c8] 8. The digital-to-analog converter of claim 1, wherein said voltage divider comprises a NFET in parallel with each said tunneling NFET.

[c9] 9. A digital-to-analog converter comprising:

a voltage source supply;

a voltage division stack connected to said voltage source supply;

a multiplexer connected to said voltage division stack;

a digital circuit connected to said multiplexer;

an analog circuit connected to said multiplexer; and

an input binary word source connected to said digital circuit;

wherein outputs of said digital circuit are input into said analog circuit and converted as analog output.

[c10] 10. The digital-to-analog converter of claim 9, wherein said multiplexer comprises any of a n-type field effect transistor (NFET), a p-type field effect transistor (PFET), and a combination thereof.

[c11] 11.The digital-to-analog converter of claim 9, further comprising a capacitor connected to said analog circuit.

[c12] 12. The digital-to-analog converter of claim 11, wherein said multiplexer and said capacitor comprise an oxide of at least 5 nm in thickness.

[c13] 13. The digital-to-analog converter of claim 9, further comprising a binary-weighted tunneling current device connected to said digital circuit.

[c14] 14. The digital-to-analog converter of claim 13, further comprising:

a node coupled to said digital circuit;

at least one current supply field effect transistor (FET) coupled to said node; and

an output FET operable for supplying a current proportional to a current of said current supply FET;

wherein said current supply FET is operable for maintaining voltage on said node constant.

[c15] 15. The digital-to-analog converter of claim 13, wherein said tunneling current device outputs tunneling current, wherein said tunneling current is adjusted in proportion to a binary weight of said input binary word source.

[c16] 16. The digital-to-analog converter of claim 9, wherein said voltage division stack comprises an NFET transistor in parallel with a tunneling NFET.

[c17] 17. The digital-to-analog converter of claim 9, wherein said digital circuit comprises a NAND device.

[c18] 18. The digital-to-analog converter of claim 9, wherein said analog circuit comprises an operational amplifier.

[c19] 19. A method of converting a digital signal into an analog signal, said method comprising:

arranging a plurality of n-type field effect transistors (NFETs) into a voltage division stack;

applying a regulated output of voltage to said voltage division stack;

applying a binary-weighted input word to a digital circuit;

applying a voltage output of said voltage division stack to each of a multiplexer and said digital circuit;

generating a digital output from said multiplexer and said digital circuit;

inputting said digital output into an analog circuit; and

converting said digital output into an analog output.

[c20] 20. The method of claim 19, further comprising connecting a binary-weighted tunneling current device to said digital circuit, wherein said tunneling current device outputs tunneling current, wherein said tunneling current is adjusted in proportion to a binary weight of said input binary word source.